5th ASCENT Newsletter –April 2017

Priority Call: 14nm PDK / virtual data

Themed Proposal Call – Q2/2017

A call for proposals targeted at researchers looking for **14nm PDK / electrical characterisation data** is currently open. These proposals will be given priority until Friday 30th June. Submission is an easy and straightforward process, click HERE for details.

This is a new extra option for researchers to engage with ASCENT. Until the end of June 2017 ASCENT will give priority to researchers interested in access to Virtual Data.

Virtual Access (VA)
Researchers can access data from both imec and CEA Leti test chips.

Test chips Documentation and Data (imec)

- FinFET and GAA test chip documentation and DATA
- III/V InGaAs GAA test chip documentation and DATA
- PLANAR test chip documentation and DATA

Material for Device Analysis (CEA-Leti)

- SPICE models and model cards for 14nm FDSOI and below.
- Process Development Kit (TCAD decks):
    - 14nm FDSOI MOSFET,
    - Trigate SOI Nanowire and
    - GAA Nanowire MOSFET (mainly electrostatics)

To gain access simply complete this enquiry form
http://www.ascent.network/contact/enquiryform/

This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.

Prof Enrique Miranda video
(Universitat Autònoma Barcelona)

Prof. Miranda visited Tyndall for a week to carry out electrical charaterisation on test chips. This short video (<2 mins) gives an insight into his work and experience of ASCENT.

https://youtu.be/zMGhRd4XXDc

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Update on activity

Since our last newsletter in January we have had a great interest in ASCENT from researchers all across the globe:

- **23 researchers** have joined the ASCENT network from 14 countries bring up our total membership to 230. Welcome to our new members from Belgium, France, Germany, India, Ireland, Israel, Italy, Japan, Netherlands, Romania, Spain, Taiwan, UK and USA!
- **17 technical enquires** have been received since January requesting access to a wide variety of facilities and expertise including access to physical characterisation equipment at Leti, access to test chips at imec, electrical characterisation of 14nm FDSOI devices at Leti, novel metal characterisation at Tyndall, novel device fabrication at Tyndall and many more enquiries that are currently being discussed and assessed by our Technical Points of Contact.
- **15 virtual access projects** are in progress giving access to Process Design Kits (PDKs) for both imec and Leti's 14nm CMOS technology as well as transistor and test structure specifications and electrical characterisation data. Our virtual access users come from countries across Europe in Armenia, Austria, Belgium, Bulgaria, France, Greece, Ireland, Romania, Spain, Switzerland and the UK.
- **17 transnational access projects** have been approved to date, 13 are in progress while 4 are complete The projects are providing researchers with a wide range of access to expertise and infrastructure including provision of test wafers, access to electrical characterisation facilities, nanofabrication facilities for novel nanoscale devices and physical characterisation facilities such as TEM and Atom Probe Tomography facilities. The ASCENT funding covers the work that is undertaken at each partner site and also the travel and expenses for the users - see our success stories on the ASCENT website:

  http://www.ascent.network/community/success-stories/
- **3 Joint Research Activities** are in progress involving the partners to investigate improved device forensic techniques, provide common data formats and benchmarking new materials for advanced 2-D materials.

Extended Offer:

- **CEA-Leti** have added Physical Characterisation systems and methods including AFM, TEM, SIMs, Atom Probe Tomography, XRD and XPS to their access offer.
- **Imec** have added 28nm test chips and VA data for finFETs, GAA and III-V GAA devices.

All the details are on the ASCENT website: http://www.ascent.network/access/

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ASCENT presentation & stand at ICMTS'17, Grenoble, France 27th-30th March

The 2017 International Conference on Microelectronic Test Structures was organised by CEA-Leti in Grenoble in collaboration with IMEP/INPG and technically co-sponsored by the IEEE Electron Devices Society.

http://icmts2017.insight-outside.fr/

The purpose of this conference is to bring together designers and test structures users to discuss recent developments and future directions of research on test structures for micro and nanoelectronics.

ASCENT was present at ICMTS'17 with an exhibitor's booth. This allowed the ASCENT team to hold one-to-one discussions with conferences attendees. ASCENT also presented their activities to the whole conference audience during the exhibitors' session. We demonstrated how ASCENT can help their research by providing access to both test chips/wafers and electrical characterisation equipment.

Several attendees signed-up to the ASCENT network following the presentation and exhibition.

Nicolás Cordero (ASCENT TPoC) presenting the programme at ICMTS'17

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