

3rd ASCENT Newsletter – September 2016

ASCENT to visit Romania: CAS 2016 – 10th to 12th October 2016

Dr Anda Mocuta, from imec in Belgium is an invited speaker at this conference and will deliver a presentation titled “Advanced CMOS devices at scaled nodes”. This talk will review transistor challenges as CMOS technologies area scaling continues. The transition between finFETs and gate-all-around nanowires is explored, and also, what choice is most suitable depending on application space – low power vs high performance. Anda will also give a short presentation about the ASCENT project and what it offers researchers, namely 14nm Datasets, Nanoscale Test Chips and Characterisation facilities. If you are attending this conference please come over to the ASCENT stand to learn more about the project and its offering. <http://www.imt.ro/cas/>



Peles Castle, Sinaia, Romania

This event is an International Semiconductor Conference (CAS 2016). The aim of the conference is to provide a forum of debate on selected topics of scientific research and technological development. On the other hand, this is an occasion for refreshing a broad perspective of the participants through invited papers and tutorials. The Conference is underlying the development in micro-and nanotechnologies, still maintaining the "traditional" connection with semiconductor electronics.

This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.

ASCENT 3rd Workshop

MOS-AK Meeting at ESSDERC 2016 (Lausanne, Switzerland)

Jim Greer presented ASCENT at the MOS-AK Workshop which took place on Monday September 12th during the ESSDERC 2016 conference.



MOS-AK aims to encourage interaction and sharing of all information related to compact modelling. It has built a community with global connections by promoting standardisation of compact models and its implementation into software tools, connecting national and local modelling groups on European level and building strong bilateral ties with similar organizations around the world. MOS-AK conducts regular meetings with European industry and academia to exchange information on the strengths and weaknesses of the industrialisation of the compact models.

The most recent MOS-AK Workshop was held on September 12th during the course of ESSDERC 2016. More than 25 attendees were shown the challenges encountered by TCAD and compact modelling specialists due to the arrival to sub-20 nm technologies. A part of the solution is a research infrastructure accessible for the global nanoelectronics modelling, characterisation and design communities. This emphasised the need for ASCENT, which provides access to characterisation facilities, test chips and virtual access to data for the 14nm finFET (imec) and FDSOI (Leti) technologies. ASCENT offers simplified access to advanced technology and research infrastructures.

As well as participating in the Workshop, ASCENT was also present at ESSDERC 2016 with an exhibition stand. There was strong interest on the ASCENT offerings, with 20 attendees signing up to become members of the ASCENT community.

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ASCENT online webinar

We are planning to host a series of webinars to engage directly with ASCENT Network Users in the modelling and characterisation community. The first webinar will take place on Thursday 6th October at 10am (Ireland).

Prof. Jim Greer (ASCENT Co-ordinator) will deliver a 30 minute presentation followed by an opportunity to engage through emailing into the session for the questions & answers...

Jim will outline the technology and infrastructure on offer at all three partner sites, imec in Belgium; CEA-Leti in France and Tyndall in Ireland while also giving examples of projects funded to date.

Contact paul.roseingrave@tyndall.ie to register for this free event. The webinar will be reached via a web browser address which will be sent to all who have registered for this event.

Thursday 6th October 2016



Time: 10:00am (WET)
11:00am (CET)
12:00 noon (EET)

Duration: 30 minutes
With Q+A afterwards

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Profile: Gilles Reibold – CEA-Leti

Gilles Reibold is the LETI Technical Point of Contact (TPOC) in the ASCENT project.

Gilles received a Ph.D. degree from the Institut National Polytechnique de Grenoble, France in 1983, on the topic of noise in MOS transistors and CCD. He joined LETI to work on development of submicron CMOS technologies, focusing on devices simulation, characterization and hot carrier effects. He was then in charge of a project in LETI aiming to develop a complete set of reliability activities, from material to circuit studies.



From 1994 to 2003 he managed an electrical characterisation group. From 2003 to 2011 he led a team focusing on electrical characterization and modelling of new technologies for CMOS and Memories, mainly around high-k materials. Since 2011 he is responsible of the Advanced Electrical Characterization Laboratory covering various electrical tests systems and Research on topics as High-k materials, SOI devices, Nanowires, Non Volatile Memories (FLASH, PCRAM, OXRAM, CBRAM), Power GaN Devices and Photovoltaic. He is co-author of more than 200 papers in these fields and is or has been committee member of P2ID, INFOS, SISC, ISAGST, IRPS and IEDM conferences. He was involved in reliability teaching, was Reliability Summer School Scientific Chair (MIGAS 1999), chairman of INFOS 2011 and will be tutorial chair of ICMTS 2017 in Grenoble.

As TPOC, his main task is to manage within the LETI requests generated by the ASCENT project. He assesses the nature of the request and decides on the appropriate resources to be engaged to respond to each request, including the CEA LETI staff to be utilized. He then interfaces with relevant technical or operational people in order to execute the User's request, facilitate user access in agreement with existing internal procedures, and guarantee a high quality level of service.

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