FROM RESEARCH TO INDUSTRY

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ASCENT PROJECT: ACCESS TO FDSOI AND NANOWIRE PLATEFORMS

ASCENT review, Leuven, May 10th 2016 – G. Reimbold, O. Faynot, D. Holden

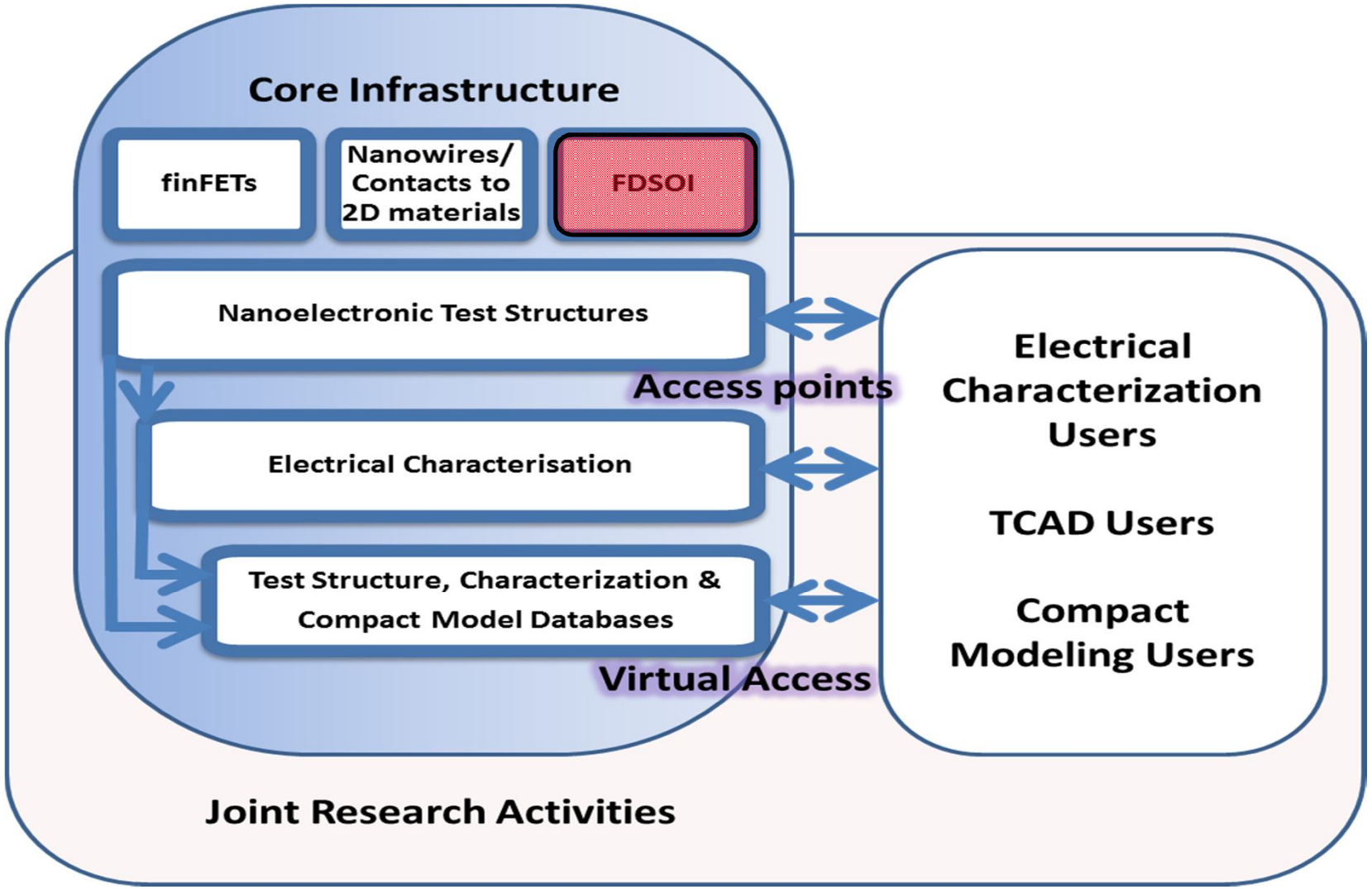
ascent

European Nanoelectronics Access

ASCENT MAIN OBJECTIVES

- **ASCENT will:**
  - Leverage Europe's Unique advantage in nanofabrication to strengthen modeling and characterisation research community
  - Accelerate development of advanced models at scales of 14nm and below
  - Provide characterisation community with access to advanced test chips, flexible fabrication and advanced test and characterisation equipment
  - Make project outputs available and easily accessible to nanoelectronics research community

ASCENT PROJECT



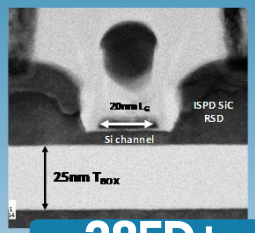
- **LETI roadmap in CMOS**
- Recent advances in planar FDSOI
- Recent advances in Nanowires
- Accessible material

ADVANCED CMOS ROADMAP

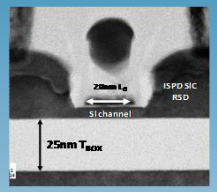
Early material and process coupling

Device scaling: technology driven performance improvement

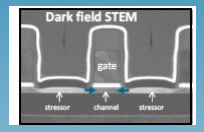
28FD

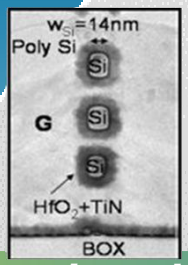


22FD



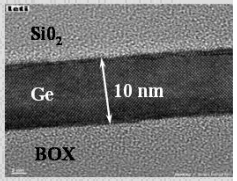
Next Gen



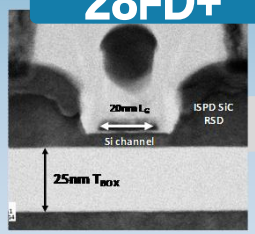


Non planar / trigate / stacked NW

High mobility materials Ge and III-V



28FD+



FinFET

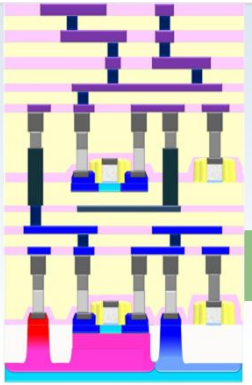
2009 — **14nm** — 2012 — **10nm** — 2015 — **7nm** — 2018 — **5nm** — 2021

Disruptive scaling

Hybrid logic

- Steep slope devices
- Mechanical switches
- Si Quantum bits

Alternative to scaling and diversification



CoolCube™ for 3D VLSI

Early design coupling

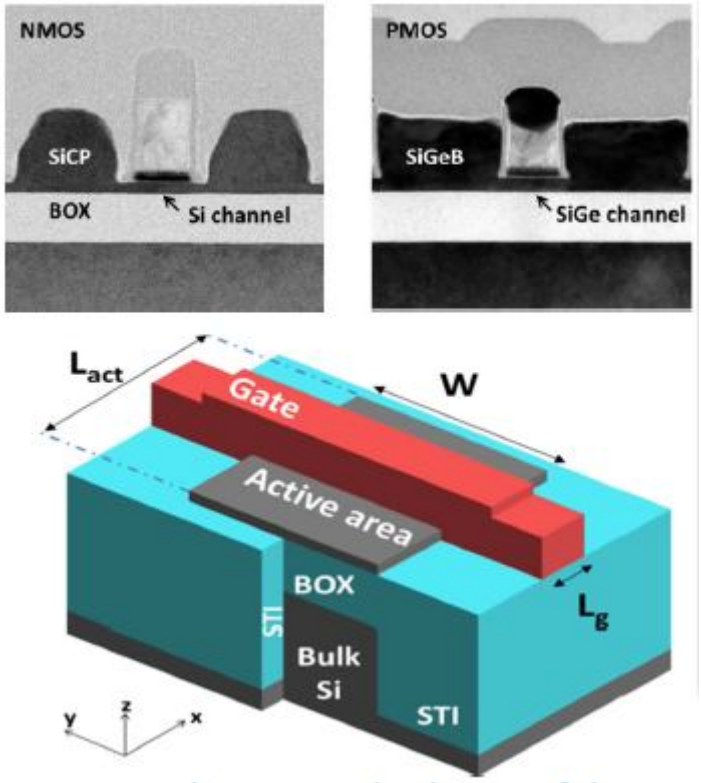
- LETI roadmap in CMOS
- **Recent advances in planar FDSOI**
- Recent advances in Nanowires
- Accessible material

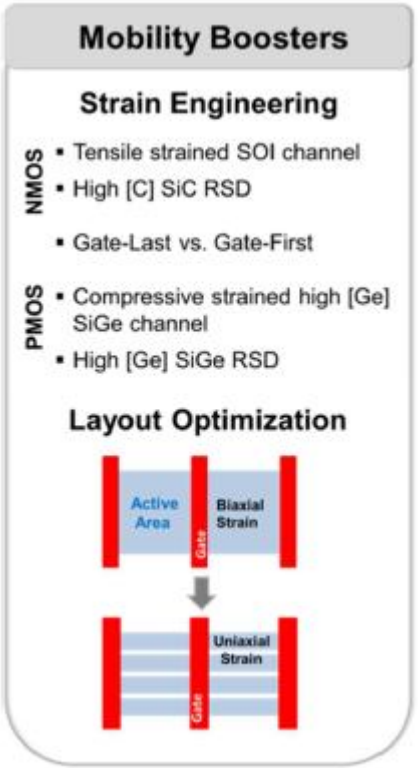
ADVANCES IN PLANAR FDSOI

MAIN CHALLENGES TODAY

- **Strain incorporation for sub14nm nodes**
  - Bi-axial NMOS / Uniaxial PMOS
- **Low temperature process to improve electrostatic control and enable 3D sequential integration**

STRAIN MANAGEMENT IN PLANAR FDSOI



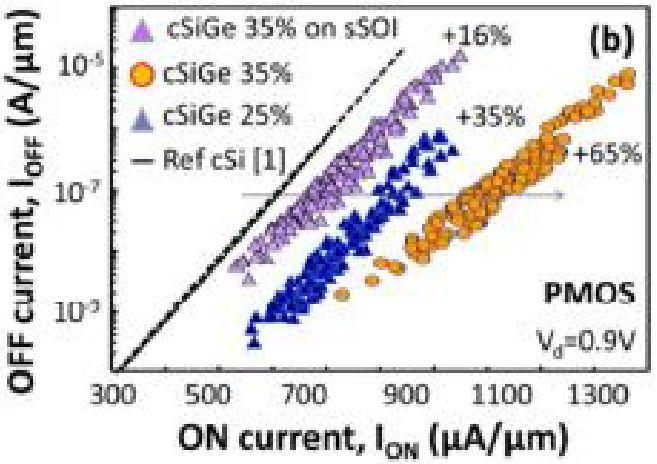


- **In depth analysis of layout effects**
- **Modeling and strain optimisation**

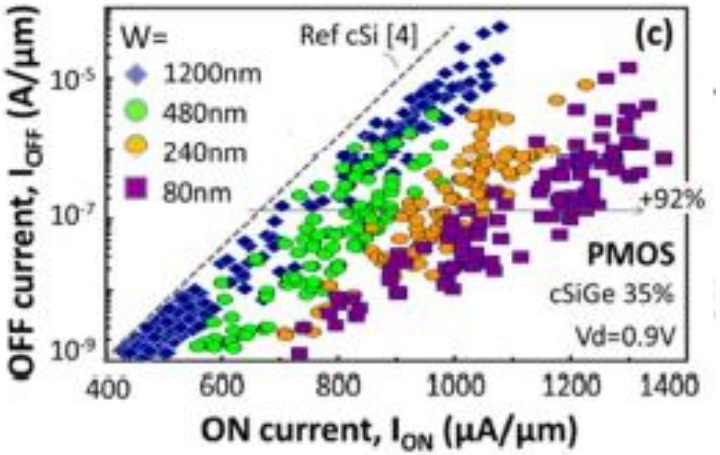
B. De Salvo, IEDM 2014, O. Weber et al, VLSI 2015

STRAIN MANAGEMENT IN PLANAR FDSOI

HIGHER SIGE FOR PMOS BOOST



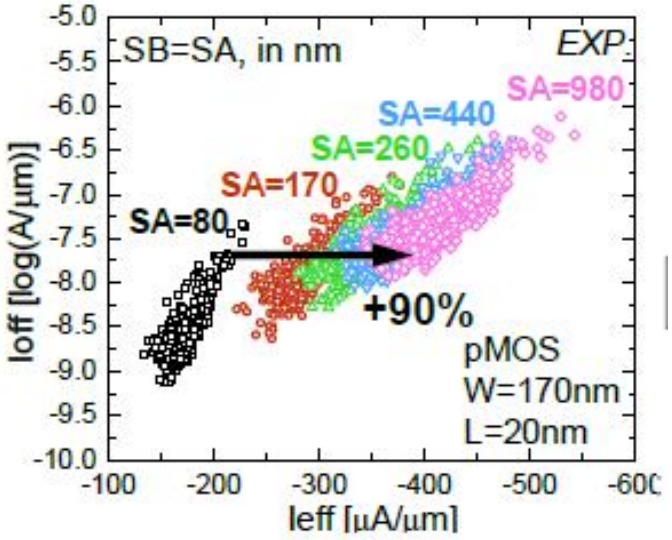
BI => UNI-AXIAL STRAIN AT SMALL W

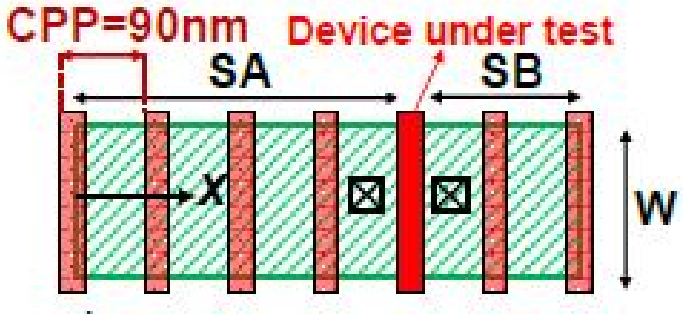


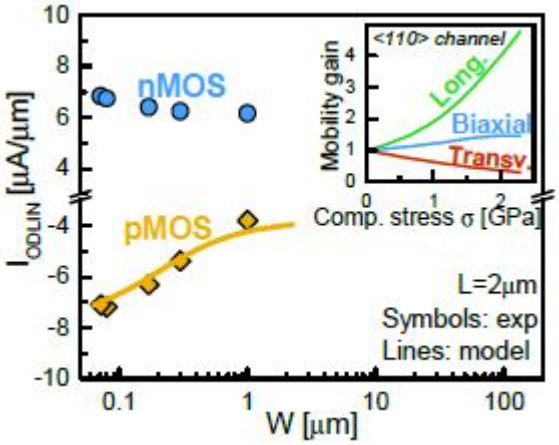
- Strong impact of device geometry
- Modeled and understood

STRAIN MANAGEMENT IN PLANAR FDSOI

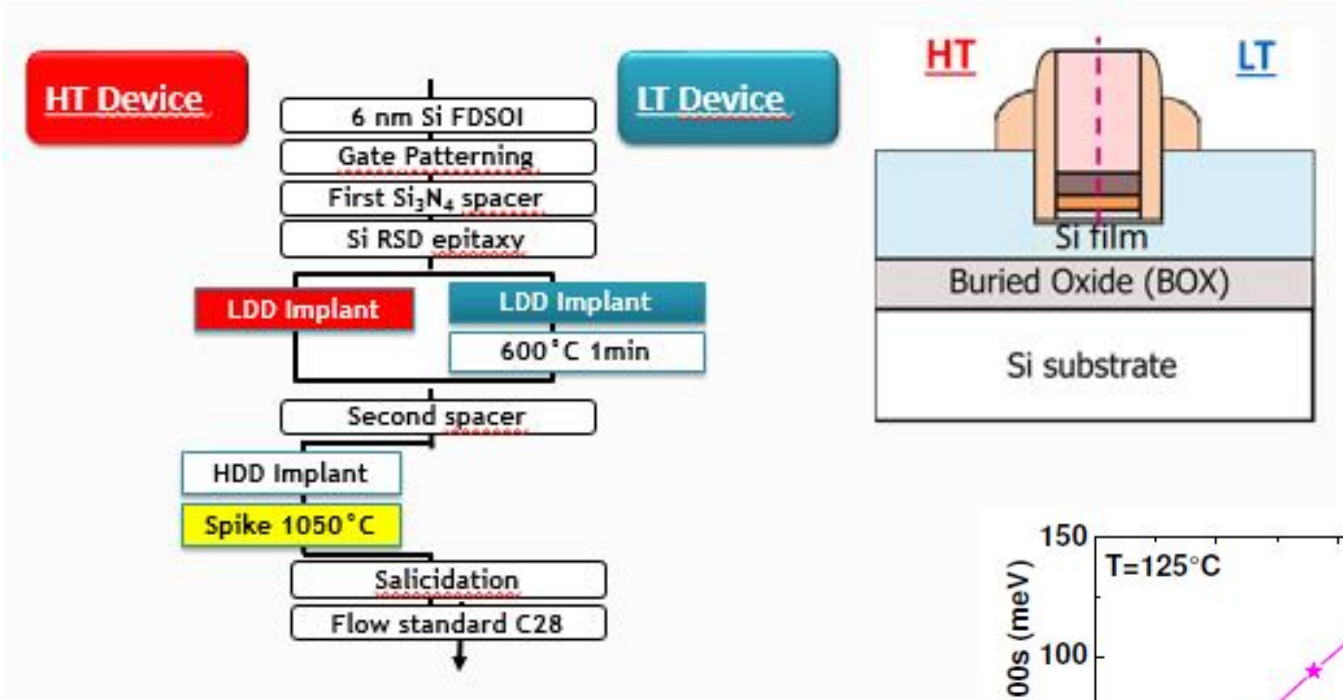
LAYOUT IMPACT

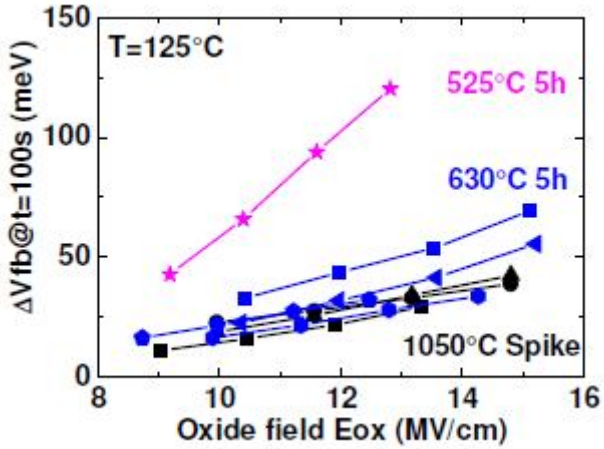






LOW TEMPERATURE PROCESS

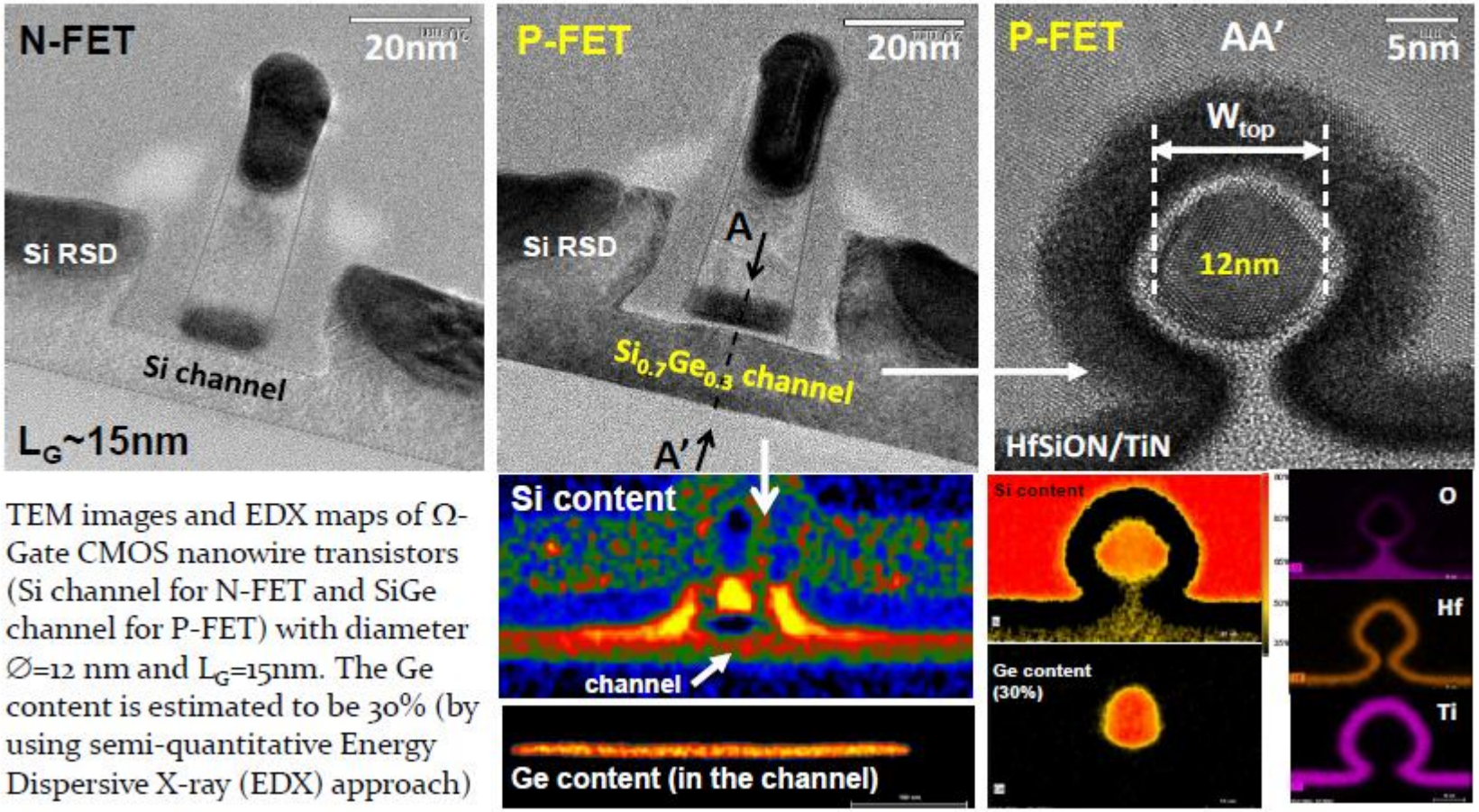




- **Key process steps identified:**
  - Gate stack (reliability)
  - Epitaxy (speed/quality)

- LETI roadmap in CMOS
- Recent advances in planar FDSOI
- **Recent advances in Nanowires**
- Accessible material

Ω-Gate CMOS Nanowire Transistors

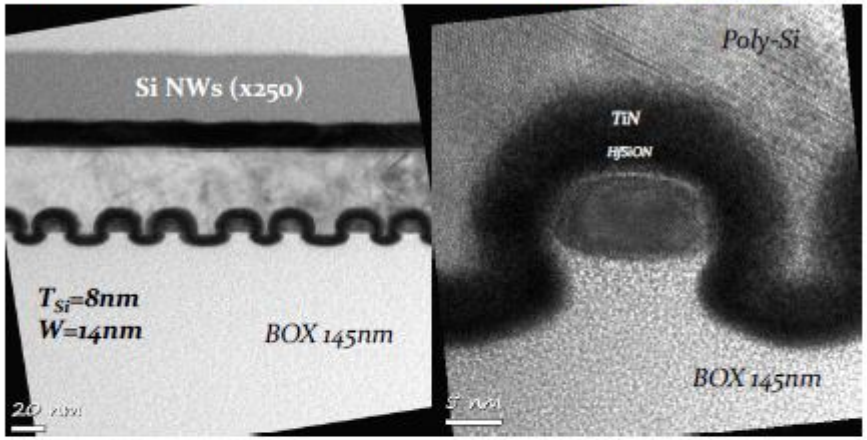


TEM images and EDX maps of Ω-Gate CMOS nanowire transistors (Si channel for N-FET and SiGe channel for P-FET) with diameter ∅=12 nm and L_G=15nm. The Ge content is estimated to be 30% (by using semi-quantitative Energy Dispersive X-ray (EDX) approach)

Advanced Patterning SIT – FP=35nm

35 nm pitch – 250channels – W=14nm, T_{Si}=8nm

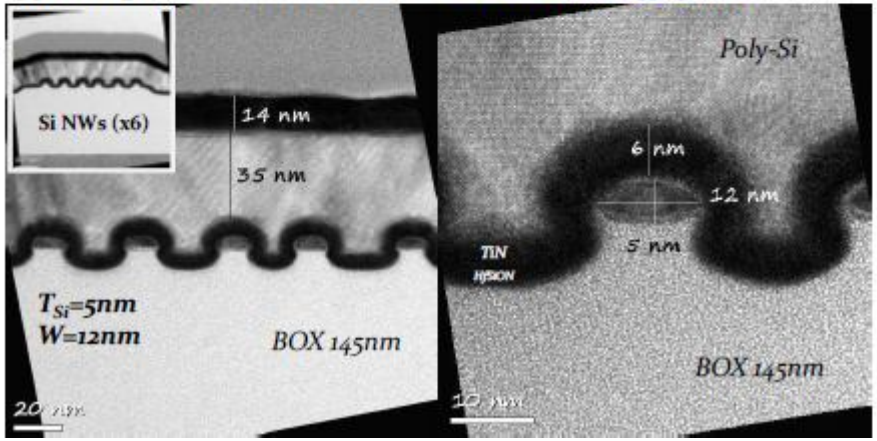
Fig. 1



- Demonstration of Ω-shaped-gate NW transistors fabricated by **SIT with a 35nm pitch**.
- An optimized SIT process has been developed to obtain either 6 or 250 wires in active area after patterning.

35 nm pitch – 6 channels – W=12nm, T_{Si}=5nm

Fig. 2



16 nm Gate Length

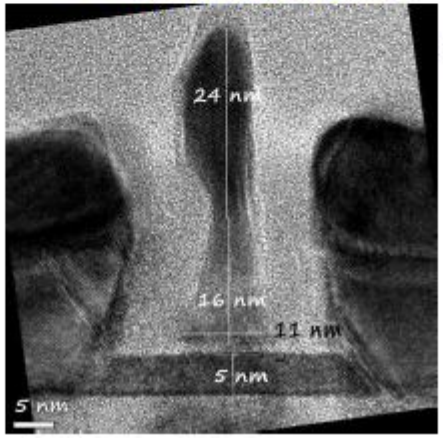
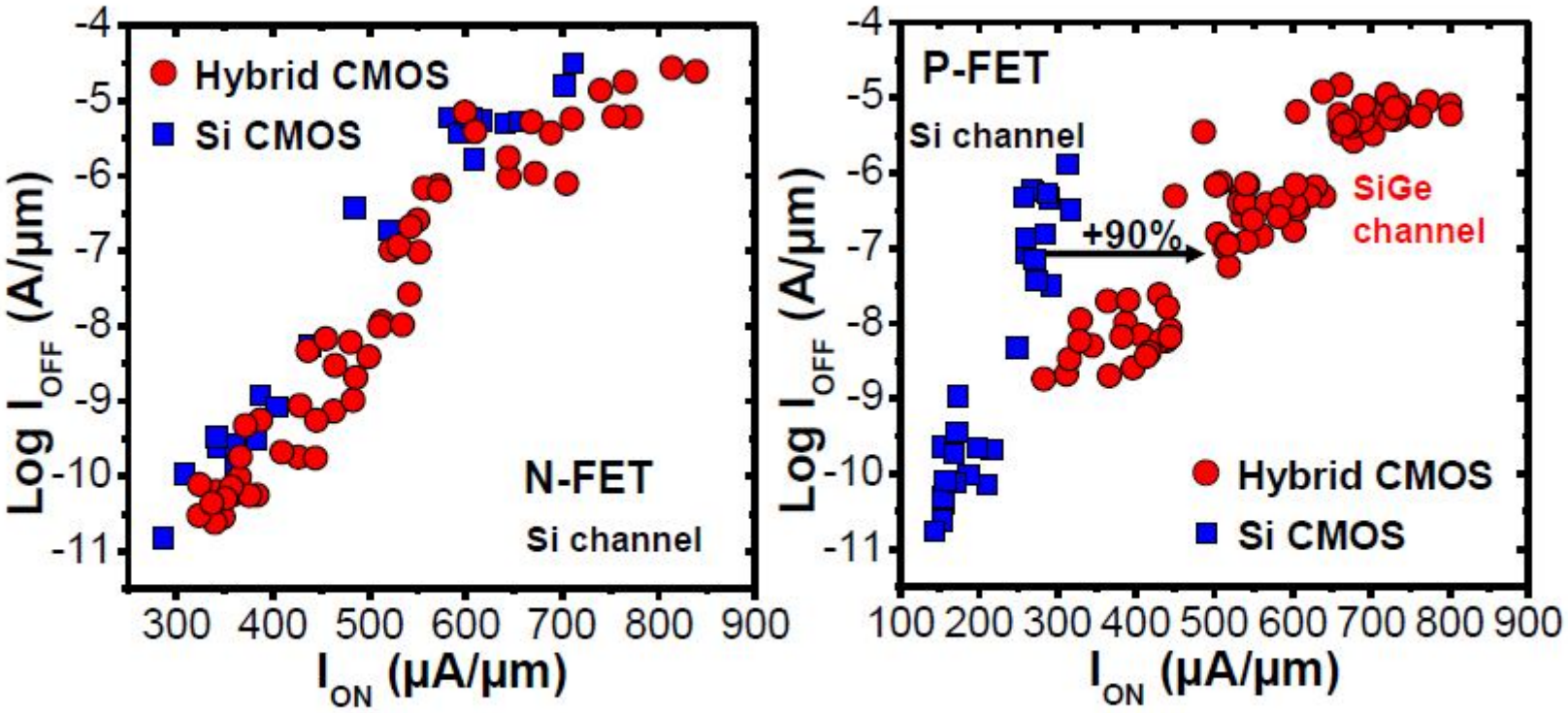


Fig. 3

Short-Channel Performance



The uniaxial compressive strain in p-FET SiGe-channel NWs results in a **+90% I_{ON} current improvement compared to Si devices** (V_{DD}=0.9V). No degradation of short-channel n-FET performance is evidenced.

- LETI roadmap in CMOS
- Recent advances in planar FDSOI
- Recent advances in Nanowires
- **Accessible material**
  - ✓ **Wafers**
  - ✓ **SPICE models**
  - ✓ **TCAD decks**
  - ✓ **PDK for Full custom IC design**
  - ✓ **Access to electrical characterization**

ACCESSIBLE MATERIAL

MATERIAL FOR DEVICE ANALYSIS

- **300mm wafers with planar FDSOI and Nanowire devices:**
  - With strain engineering
  - With low temperature processes

- **SPICE models and model cards for digital design:**
  - 14nm FDSOI PRELIMINARY
  - 10nm FDSOI TARGET
  - 10nm FFSOI TARGET

- **TCAD decks (electrical):**
  - FDSOI MOSFET
  - Trigate SOI Nanowire
  - GAA Nanowire MOSFET

- **To come in the near future: (Q2 2016)**
  - Spice model for Stacked NWs (7nm tech. node) TARGET

ACCESSIBLE MATERIAL

MATERIAL FOR CIRCUIT PERFORMANCE ANALYSIS

- **Preliminary PDK for Full custom IC design:**
  - 14nm planar FDSOI technology PRELIMINARY
  - 10nm planar FDSOI technology PRELIMINARY

- **Near future (Q2 2016)**
  - PDK 10nm including libraries PRELIMINARY

Contact Person @LETI: D. Holden (david.holden@cea.fr)

INDICATIVE STANDARD CELLS LIB.

COMBINATIONAL CELLS				
Cell Name	#In	Description	Drive Strengths	#Cells
BUF	1	Buffer cells	X1 to X16	6
INV	1	Inverter cells	X1 to X16	6
AND	2, 3 and 4	AND cells	X1 and X2	6
OR	2, 3 and 4	OR cells	X1 and X2	6
NAND	2, 3 and 4	NAND cells	X1 and X2	6
NOR	2, 3 and 4	NOR cells	X1 and X2	6
MUX2	3	Multiplexer cell	X1	1
XOR	2	XOR cell	X1	1
XNOR	2	XNOR cell	X1	1
AOI	3 and 4	AND-OR-Inverter cells	X1 and X2	4
OAI	3 and 4	OR-AND-Inverter cells	X1 and X2	4
FA	3	Full-adder cell	X1	1
HA	2	Half-adder cell	X1	1
			TOTAL	**49**

SEQUENTIAL CELLS				
Cell Name	#In	Description	Drive Strengths	#Cells
DFFRNQ	3	D flip-flop with asynchronous !reset	X1	1
DFFSNQ	3	D flip-flop with asynchronous !set	X1	1
SDFFRNQ	5	D flip-flop with scan and asynchronous !reset	X1	1
SDFFSNQ	5	D flip-flop with scan and asynchronous !set	X1	1
LHQ	2	High enable Latch	X1	1
			TOTAL	**5**

CLK CELLS				
Cell Name	#In	Description	Drive Strengths	#Cells
CLKBUF	2	Clock buffer cells	X1 to X16	6
CLKGATETST	3	Clock gate with test pin	X1	1
			TOTAL	**7**

ACCESS TO THE ELECTRICAL CHARACTERIZATION INFRASTRUCTURE

- **Laboratory size: 450 m²**

ELECTRICAL CHARACTERIZATION (1)

Available systems and methods

- ✓ Parametric testers with 300mm full auto probers
- ✓ Probe cards and new membrane cards
- ✓ Statistical data treatment
- ✓ Functional tests
- ✓ General purpose I(V)-C(V) 200/300mm testers
- ✓ Temperature range for test on wafers 2°K => 600°C
- ✓ Test systems for memories
- ✓ HF tests up to 40 MHz
- ✓ Noise measurements

ELECTRICAL CHARACTERIZATION (2)

- ✓ Reliability tests: hot carriers, TDDB, charge pumping,…
- ✓ Internal Photo Emission
- ✓ Emission microscopy (visible & infrared)
- ✓ Electrical test under calibrated strain
- ✓ High power tests (10kV, > 100A) on 300mm prober
- ✓ Deep Level Transient Spectroscopy
- ✓ Electrostatic discharges
- ✓ Electromigration
- ✓ Oven and climatic environments

Thanks and wellcome in LETI