

8th ASCENT Newsletter – January 2018

#1 imec Report: 1st PhD Accelerator Programme



Left to right: Nicolo Zagni (Univ Modena & Reggio Emilia), Mandar Suresh Bhoir (Gandhinagar IT), Theodoros Oproglidis (Aristotle Univ Thessaloniki), Artemisia Tsiara (CEA-Leti), Laura Zurauskaite (KTH Stockholm) & Krishna Pradeep (Univ Grenoble Alps)

On November 20th 2017 imec hosted the very first ASCENT PhD Accelerator workshop. Various topics were covered addressing reliability and failure mechanisms in state-of-the art microelectronic devices. This gave the opportunity to 6 international students, selected by the 3 institutes from a pool of ~40 applicants interested to step in the ASCENT project, to get insights in dielectric breakdown, self-heating, back-end reliability, etc.

This unique 4-day workshop, organized by the imec academy, was used as a stepping stone to promote the interactions between PhD students, experts and also to offer greater visibility on potential ASCENT partnerships. Dedicated discussions were scheduled between the students and the imec points of contact.

This very successful event already triggered three (50% of the total) user enquiries within the first 3 weeks after workshop completion, confirming interest from the international community and indicating that promotion and dissemination is key in such international collaboration.

This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.



Presentations were delivered at the imec Academy

This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.



Funded by the European Union

#2 CEA Leti & Tyndall Accelerator Programme news

2nd Call - CEA Leti: This call, which closed on 15th Dec 2017, attracted a large number of applications from across Europe and beyond. The results of this call will be announced later this week when all applicants will be contacted by email. The programme will be delivered from 5th-7th March 2018 in Grenoble, France.

3rd Call - Tyndall National Institute: This call will be announced shortly.

This programme will again feature a three day visit to Tyndall in Ireland for PhD students. During the visit attendees will be introduced to both the theoretical and practical aspects of nanoelectronics and nano-fabrication techniques (including e-beam lithography). Electrical (RF, etc.) and physical characterisation (TEM, SEM, AFM, etc.) techniques will be covered in some detail to demonstrate the various aspects of the ASCENT offering.



This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.

#3 Access to imec FinFET Electrical Characterisation Data

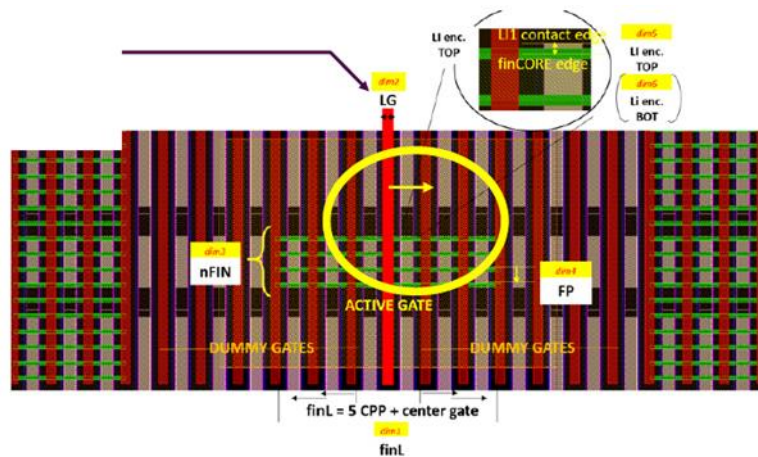
The imec contribution to the Virtual Access area of the ASCENT project is multi-fold. First of all, 14nm bulk finFET state-of-the-art device characteristics for both nMOS and pMOS devices are available. These cover a range of bias conditions and device geometries. Alternatively, temperature dependence could be offered as well.

A similar set of characteristics is also partially available for gate all around (GAA) silicon nanowire as well as III-V nMOS devices. The offering is not limited to the above mentioned technologies and is tuned to the requestor's needs. Data collected in the transnational access projects are also added to the database, for example, we have included variability results aiming at mismatch analysis on 14nm silicon bulk finFET devices.

ASCENT also offers test chip documentation and electrical characterisation data for [imec's](#) technologies:

- 14nm FinFET and silicon gate-all-around (GAA) devices
- III/V InGaAs GAA
- Planar 28nm

To access this data, just submit an enquiry ([ASCENT Enquiry Form](#)) describing your requirements and our team will take you through the registration process.

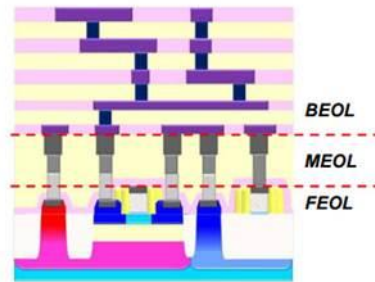


This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.

#4 Access to Leti FDSOI Process Development Kit (PDK)

ASCENT also offers access to process development kit (TCAD decks) for [Leti's](#) 14nm FDSOI technology, tri-gate SOI nanowires and GAA Nanowires. This PDK includes SPICE models and model cards.

To access the PDK, just submit an enquiry ([ASCENT Enquiry Form](#)) describing your requirements and our team will take you through the registration process.



This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.

#5 New 2018 Webinar series

We host webinars directly with researchers that are interested in learning about how they can access research infrastructure through the ASCENT programme.

The ASCENT team at Tyndall National Institute (Ireland) will arrange a suitable time with you and we will deliver a 30 minute presentation followed by an opportunity for a Q & A session.

We will outline the technology and infrastructure on offer at all three partner sites, at imec in Belgium, CEA-Leti in France and Tyndall in Ireland, while also giving examples of projects which have already been delivered through the programme.



Date & time: To suit you
Purpose: Information on offerings
Duration: 30 minutes
Q&A: Afterwards

Contact [paul.roseingrave \(at\) tyndall.ie](mailto:paul.roseingrave@tyndall.ie) to arrange your own group webinar.

This project has received funding from the *European Union's Horizon 2020 research and innovation programme* under grant agreement No 654384.