ASCENT PARTNER MEETING

WP6: Access to finFET Technology

T. Chiarella, A. Mocuta, J. Mitard, V. Terzieva

10/05/2016 Leuven, Belgium
Workshop Agenda

1) ASCENT: An EU initiative for access to Nanoelectronics Infrastructure – Prof. Jim Greer (Tyndall National Institute, Ireland)

2) Tyndall: Accessing flexible nanoelectronics fabrication at Tyndall – Dr Graeme Maxwell (Tyndall)

3) imec: Advances and Access to FinFET Technology – Thomas Chiarella (imec, Belgium)

4) Virtual Access to advanced device data – Thomas Chiarella (imec, Belgium)

5) Leti: Advances and Access to planar FDSOI and nanowire structures – Dr Olivier Faynot (CEA-Leti, France)

6) ASCENT access: User perspective - Prof. George Angelov (Technical University of Sofia, Bulgaria)

7) Q&A session
ASCENT - Access to European Nanoelectronics Network

- Provide advanced test structures to the European research and academic community.
- To foster the growth of a research community about the ASCENT research infrastructure
- To accelerate the development of advanced technology computer aided design models and tools
- To enable the systematic characterization of physical and processing effects arising below 10 nm
- To make all outputs easily accessible to the nanoelectronics community through a single access portal

The infrastructure providers in the ASCENT consortium are Tyndall (IE), Imec (BE), and CEALETI (FR)
UNIQUE HIGH-TECH INFRASTRUCTURE

Nanofabrication Facilities (Lab + 300mm Fab)
- 4800 m² Class -1000 Clean Room
- Next-Gen. patterning capability (Eg. EUV)
- Advanced Materials Flexible (Eg. III-V + Si capable)
71 DIFFERENT NATIONALITIES IN 2014

+ 1,177 Belgians
+ 169 Dutch
FULL ECO SYSTEM

UNIVERSITIES

IMEC

EUROPE

GOVERNMENT

INDUSTRY
ACCESS TO SI BULK FINFETS STRUCTURES

Objectives

- Provide the **technology elements** and **electrical data** for Silicon bulk FinFETs devices
- **Advanced device characterization** for European researchers that need access to state-of-the art devices
- Provide **Si Bulk FinFETs technology data for 14nm node and below**
- Provide **Si Bulk FinFETs test structures**
Material for Device Analysis

- 300mm wafers with Bulk FinFET devices
- Silicon EPI nFET/pFET CMOS fully integrated vehicle
- Embedded SiP / SiGe S/D CMOS fully integrated vehicle
- Replacement Metal Gate [RMS] with Local Interconnect
- Single level BEOL metal

**IMEC’S OFFER**

**FinFET test chip documentation**

- Documentation of process assumptions for the test chips
- Inventory of test structure types available on the test chips
- Access to test structures data

**Electrical Characterization Capabilities**

Available systems and methods:

- >500 m² of test labs, ~25 semi-auto/manual 300mm probers
- Statistical data treatment in JMP
- Fully automatic 300mm parametric testers
- Semi-automatic 300mm parametric testers
- Temperature range for test on wafers 77/10K → high T
- Fast Pulse testing, Self-Heating characterization
- HF tests up to 50 GHz
- Noise measurements
- Reliability tests hot carriers, TDDB, charge pumping, etc.
- High power tests (1 kW, >100A) on 300mm prober
- Electrostatic discharge LAB

**Scientific & technical support**

Whenever necessary and upon request of the User, imec can offer scientific support for in-depth data interpretation.
ACCESS TO STATE OF THE ART PROCESS TECHNOLOGY

N14 test vehicle

- Fin & STI module
- NFET wells I/I
- PFET wells I/I
- Well RTA
- Dummy gate
- NFET extension I/I
- PFET extension I/I
- Extension RTA
- NFET SiN dep & etch
- NFET recess
- NFET epi
- PFET SiN dep & etch
- PFET recess
- PFET epi
- Laser anneal
- ILD0
- RMG
- Li and BEOL

State-of-the-art devices with dedicated experiments ready on 300mm Silicon wafers.

Main features: Bulk finFET, Replacement Metal Gate, S/D epi with Local Interconnect and silicide-last integration using single metal BEOL
IMEC’S EXPERTISE IN TEST/CHARAC

Imec’s expertise includes, in a nutshell, for finFET characterization:

| ✓  | Device/Layout effects |
| ✓  | Gate stack characterization |
| ✓  | Reliability [BTI/TDDB/HC...] |
| ✓  | Variability |
| ✓  | Analog / RF |
| ✓  | ESD |
| ✓  | Self-Heating |
| ✓  | Noise |
| ✓  | Temperature dependencies |
| ✓  | ... |

Current status includes sharing eTest data, mismatch results as well as silicon wafers for on-site measurements.
SUMMARY OF ACCESS REQUESTS

Currently: access and inquiries

<table>
<thead>
<tr>
<th>Ref No</th>
<th>Postcode</th>
<th>Country</th>
<th>Enquiry</th>
<th>How did you hear about ASCENT?</th>
<th>Ref No</th>
<th>Status</th>
<th>Change from last week</th>
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<tbody>
<tr>
<td>030</td>
<td>18071</td>
<td>Spain</td>
<td>Access to experimental data and models.</td>
<td>Transnational Access Ref No 010</td>
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<td>037</td>
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<td>Spain</td>
<td>Dear Sir/Madam</td>
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<td>Greece</td>
<td>In agreement with IMEC (Thomas Chiarella) we would like to get access to matching pair results in the YA framework from IMEC FinFETs on 11</td>
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<td>Dear Sir</td>
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<td>Discussions</td>
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<td>033</td>
<td>12028</td>
<td>Bulgaria</td>
<td>We would like to fabricate a prototype of an acoustic tweezers using standing</td>
<td>Heard from imec colleagues</td>
<td>033</td>
<td>VA User</td>
<td>Waiting for T&amp;C</td>
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<td>031</td>
<td>52440</td>
<td>Italy</td>
<td>I am working with imec, and would like to make a quantitative study on device</td>
<td>from co-worker in imec</td>
<td>031</td>
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<tr>
<td>032</td>
<td>3011</td>
<td>Belgium</td>
<td>なりたけら</td>
<td>Let's talk</td>
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<td>CLOSED</td>
<td>Close, No transnational</td>
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<td>Dear Sir/Madam</td>
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<td>Tyndall</td>
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<td>029</td>
<td>72250</td>
<td>Netherlands</td>
<td>We are working on monolayer doping technique which has an benefit over</td>
<td>message from Tyndall</td>
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<td>028</td>
<td>80023</td>
<td>Romania</td>
<td>Preparation and characterization of thin insulator films for TCO applications</td>
<td>very good</td>
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<td>QM is supplier of material used since 2013 to the semiconductor industry</td>
<td>from a colleague Dr. Mircea Modrea</td>
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<td>I am just finding out about Ascent, and since I work in the RF and Microwave fields,</td>
<td>through a colleague.</td>
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<td>Phase 1 finished</td>
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<td>My field of interest is doping of semiconductors (mainly In, GaAs) both bulk and</td>
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<td>Tyndall</td>
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<td>Offered VA</td>
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<td>Offered VA</td>
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<td>Graphene monolayers and TMD monolayers (MoS2, hBN, MoSe2, WSe2, ...) by CVD on</td>
<td>Invitation from Dr. Olivier Faynot (LETI)</td>
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<td>Tyndall</td>
<td>Proposal on hold</td>
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<td>1423</td>
<td>Bulgaria</td>
<td>Dear Sir</td>
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<td>Ireland</td>
<td>HI, By Dr. Ronan Farrell</td>
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<td>VA User</td>
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<td>005</td>
<td>1000</td>
<td>France</td>
<td>HN, and nanoelectronics</td>
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<td>Close, Out of Scope</td>
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<td>004</td>
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<td>France</td>
<td>As equipment supplier, we would like to run dedicated set of experiments to</td>
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<td>003</td>
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<td>Sweden</td>
<td>We are interested in knowing more about the program how it's used</td>
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<td>003</td>
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<td>002</td>
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<td>Bulgaria</td>
<td>Wanted to know if he will have to wait to have test devices fabricated or if there's test</td>
<td>e-mail to Juilee Gore</td>
<td>002</td>
<td>VA User</td>
<td></td>
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<td>001</td>
<td>12028</td>
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<td>Has an idea to contact graphene/TMC. We told him to contact you straight away.</td>
<td></td>
<td>001</td>
<td>Wait for user</td>
<td>No</td>
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</table>
Mask-set description

Added to the Flexilearn website

Data set description
+ sample charts

Device options overview

DATA COLLECTION

FILE FORMAT

1. Mos_i4_vgs

returns 4 terminal currents in ID/ID/IB/IG vs.VG AND VB

Example chart

Variation in LG
Gate to CT fixed
CPP fixed

DATA COLLECTION DOCUMENTATION
N and PFN device layout options

NFET DESCRIBED

1. Description TYPE 1 : LA – Length array within pitch
VA FINFET_IMEC

finFET_imec
Data for imec’s finFET technology

- Bulk finFET DESCRIPTION
- Bulk finFET DATA
  - Datafiles - Full Curves: IDVG/IDVD on NFIN/PFIN
- Bulk finFET Matching DATA
  - Matching Data - Full curves and VT

✓ Description provided for test structures
✓ Bulk finFET data available
  - IDVG IDVD @ RT
  - NEXT: 50C data
✓ Bulk finFET mismatch data available
  - Match pair IDVG
  - Data including VT extraction
VIRTUAL ACCESS STATUS

- 1st request: Mismatch data shared, 1st results available
- Other requests coming in, in discussion

Benchmarking FinFETs vs FDSOI nMOS

Drain current local/global variability in n and p MOS
14nm FinFETs/IMEC

T. Karatsori, C. Theodorou, R. Lavieville, G. Ghibaudo
IMEP-LAHC, Univ. Grenoble Alpes, Minatec/INPG, 38000 Grenoble, France
INQUIRY FOR BULK FINFET

- Material transfer agreement available
- Shipping wafers, project ‘start’ [3months tests]
CONCLUSIONS

▸ **ASCENT** offers great opportunity for EU researchers to reach industry relevant technology/results.

▸ **IMEC** offers
  - unique high-tech **infrastructure**
  - access to **bulk finFET** state-of-the-art devices
  - access to dedicated **test structures/test equipment and data**
STATUS

- System is in place for **data sharing**
  - Documentation and data posted on ASCENT web site [FlexiLearn]
- **VA (virtual access) is successful**
  - 1st report delivered
  - To be reviewed internally and shared back to ASCENT [VA]
- **Partners inquiry** on track
  - Silicon bulk finFET wafers shared for variability and noise studies
  - Measurements to be performed at the requestor’s site
Thank you!

Contacts: T. Chiarella
          V. Terzieva
          J. Mitard

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Jerome.Mitard@imec.be

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